

Implementation of Solder-bead Probing in High Volume Manufacturing

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Implementation of Solder-bead Probing in High Volume Manufacturing

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Abstract

Solder-bead probing is a test technology primarily targeting high-speed/high-density printed circuit boards. It is a promising complement to traditional probing solutions, because test access points are placed directly on board traces, thus addressing shrinking board real estate without compromising test quality. This paper summarizes the design, manufacturing, and test parameters Intel will use to implement the technology in a high volume manufacturing environment.

1 Introduction

Solder-bead probing was introduced to the industry by Ken Parker of Agilent Technologies at the IEEE International Test Conference (ITC) of 2004 [1]. The technology combines a new test point placement method with a well-known probing technique: The test point is placed on the PCB by opening up the solder mask and exposing the copper trace. Solder paste is applied along the trace and reflowed. The resulting solder-beads are probed at in-circuit test (ICT) using traditional bed-of-nails fixtures that have been fitted with flat-headed rather than pointed probes. [Figure 1](#) shows a graphic representation of the bead on the trace from both end and side views.

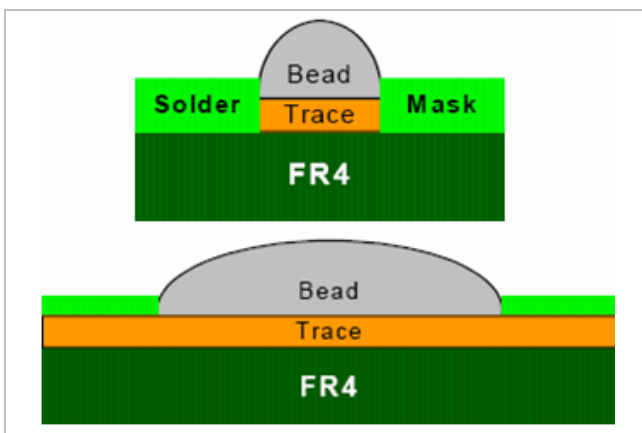


Figure 1. Top: Latitudinal or end view of bead on trace
Bottom: Longitudinal or side view

Solder-bead probing offers potential improvements for both design and test. While traditional testpoints require additional board real estate, solder beads are in-line with existing traces providing direct access to board circuitry without the need to route dedicated test circuits. This increases design flexibility, speeds up the layout process, and makes it possible to add testpoints without changing the layout. [2]

From a test perspective, increased options for nodal access means that a degradation of test quality is not a necessary consequence of higher density/higher speed PCB designs. And, if a trace has multiple access points, fixture development software can automatically select the best probe location.

The success of solder-bead probing depends on whether it can perform as well or better than traditional methods in high volume manufacturing (HVM). This paper summarizes Intel's study of the design, manufacturing, and test parameters needed for a successful implementation.

2 Design of Experiment (DOE)

2.1 Test Vehicles (TV)

Two test boards, TV1 and TV2, were designed to evaluate the parameters studied. Both had Immersion Silver (ImAg) finishes. Each board contained 3,168 beads distributed on both sides of the boards. Four-wire Kelvin measurements were provided for all solder beads. The design included two solder-bead types: metal-defined, a typical bead on a trace, and solder mask-defined, a typical bead on a power plane.

Solder mask openings were rotated at 0, 45, 90 and 135 degrees. Solder mask offset errors of +/- 3 mils, an industry specification, were introduced, using a laser etch process. Solder beads were placed on both sides to test the impact of several solder reflows. Combinations of trace widths (3-6 mils), trace spacing (4-6 mils), solder mask opening lengths (15, 20, and 25 mils), solder mask heights and various opening widths were included.

[Figure 2](#) shows solder beads on metal-defined pads on two parallel traces. Note the various rotations of the solder beads.

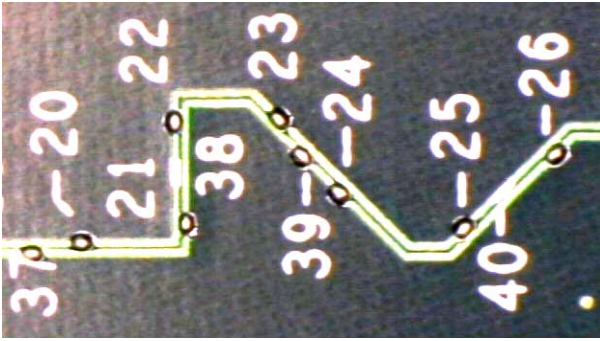


Figure 2. Metal-defined solder bead pads

Figure 3 shows solder beads on solder mask-defined pads. Note the various rotations of the solder beads.



Figure 3. Solder mask-defined solder bead pads

2.2 Research Limitations

Sample size

It is impossible to claim 100% statistical validity due to the limited volumes used in this set of experiments. While over 1.5 million beads were created and studied, this number was divided into subsets which were subjected to common experimental variables. Although this reduced the lot size of each experiment, the overall sample size warrants a high level of confidence based on the number of solder beads on each TV together with the number of tests conducted.

Scope

This study only included materials used in motherboard SMT manufacturing technologies such as FR4, an epoxy based laminate. It did not consider flex circuits or Bismaleimide-Triazine (BT), a resin based substrate.

3 Parameters Studied

3.1 Signal Integrity

Design rules can preclude the placement of traditional testpoints on high speed signal circuits. (See figures 18-21 in [1].) Though the test coverage lost at ICT can be recovered using other methods such as X-Ray or boundary scan (IEEE 1149.6), none of the alternatives offers a full solution. X-Ray can add cost, and boundary scan will not work when the chain is broken by a signal going off the board to a connector or socket, as is the case for components (CPU, memory, IO cards) that are typically not populated at ICT on computer motherboards.

If it can be demonstrated that solder-bead testpoints do not alter signal line characteristics, then test access can be added back into high speed signals, thus increasing coverage or extending the capability to continue probing buses as speeds increase.

Goal

Determine the impact of solder beads on trace performance by measuring transmission frequency with and without beads.

Test Method

A vector network analyzer (VNA) was used to inject swept sinusoidal frequencies and analyze signals on two trace sizes, 2.5 and 5.0 inches long. These were controlled for a trace impedance of 50 ohms. Solder mask openings facilitated the placement of 15 beads on the 2.5-inch trace and 30 beads on the 5-inch trace. These numbers far exceeded any realistic worst-case condition, but beads were incrementally added to determine if there was a “break point” at which an impact could be observed. Three traces of each configuration were tested up to a frequency of 20 GHz.

Results

Figure 4 shows that no discernable differences were measured between bead-less traces, represented by the blue line and those with beads, represented by the red line. Similar results were achieved with the 5-inch trace with 30 beads. We concluded that there was no risk to signal integrity up to a frequency of 20 GHz, working within the current board constraints. A break point was not observed for either the 15 or 30-bead test case.

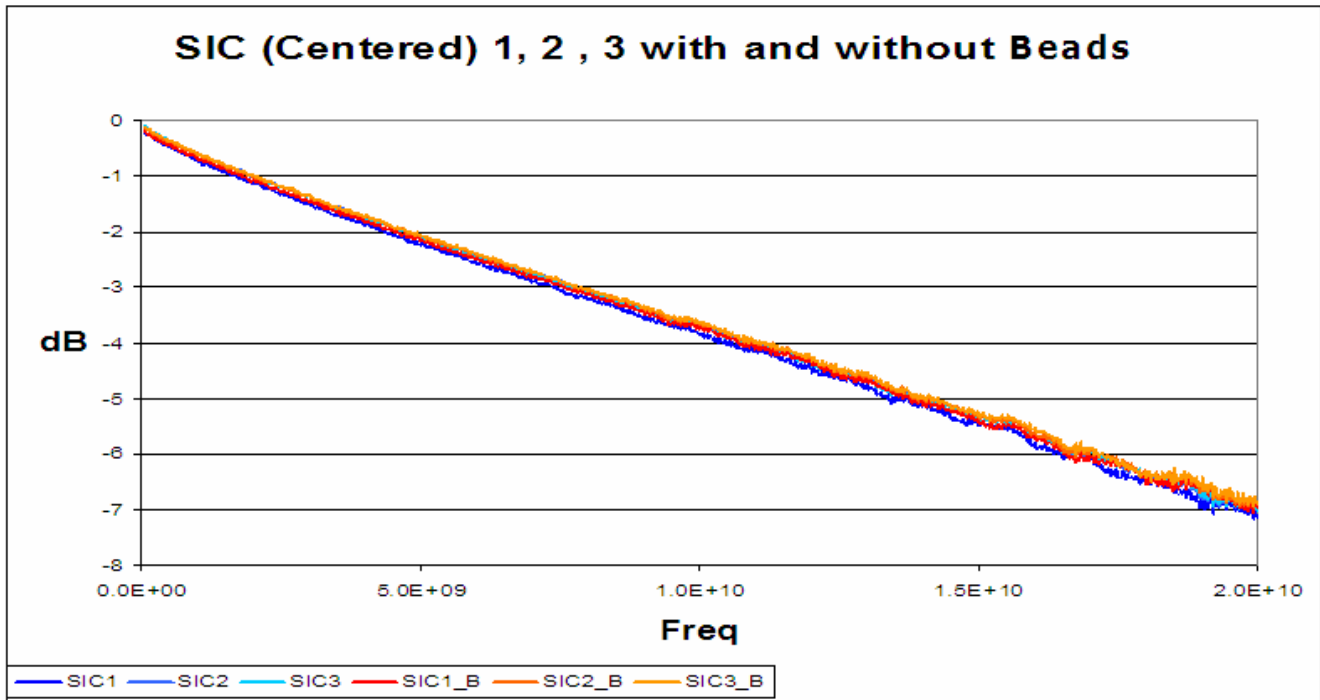


Figure 4. 2.5-inch trace with and without beads at 20 GHz

3.2 Solder Mask

One function of the solder mask is to prevent solder bridging between adjacent traces on the PCB. The size of the solder mask opening as well as its position on the trace is therefore critical. The industry standard for a finished board allows a maximum nominal clearance of 3 mils (0.003”) per side around any solderable surface.

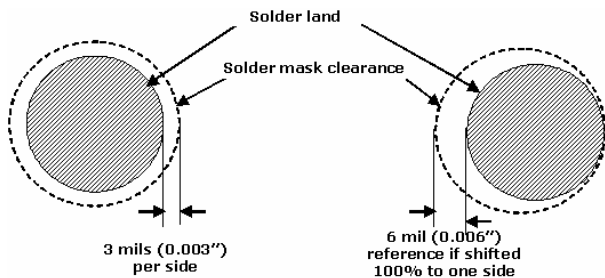


Figure 5. Solder mask registration tolerances

Worst-case misregistration can cause manufacturing defects or false test results if the opening size and shape are not selected properly: Shorts can develop between traces causing a defect, or an opening that exposes too little solderable surface to form a probeable solder bead can result in a contact failure.

Goal

Determine the optimal shape and size of solder mask openings that will yield 100% success in solder bead placement without impacting assembly processes or PCB cost.

Test Methods

Three different solder paste apertures were used: circular, square, and rectangular. Solder mask openings were all rectangular, but various widths and lengths were used.

Registration errors were deliberately injected to simulate the worst-case variability of a low-cost supplier. The process used to introduce this variance was not standard but devised only for experimental purposes: Solder mask was ablated from the top surface of the traces using a laser etcher with 40 microns of positioning accuracy. This ensured that tests reflected the outer limits of solder mask registration specifications.

Results

Square solder paste apertures compensated most effectively for misregistration in the solder paste printing process.

The length of the solder mask opening had no negative impact, but the width proved to be critical. Ideal widths were determined for various trace widths and spaces. Problems were observed with widths that were too wide or too narrow. Wider openings exposed adjacent traces allowing beads to contact more than one trace, resulting in shorts.

Smaller openings yielded contact failures: Solder beads formed on the trace, but the bond between trace and bead was inadequate. Beads were either knocked off when probed at ICT or did not make contact with the exposed trace. In some cases, the bead formed on the solder mask, due to the combination of misregistration and inadequate trace exposure.

3.3 Solder Application Technology

Reflow soldering was adopted to form solder beads throughout this study. Wave solder was predictably not viable, but preliminary experiments were performed to confirm that the mask opening would be too small to build a probeable bead. In fact, the solder formed by the wave process was not high enough to rise above the solder mask.

Boards with beads formed by reflow soldering were also sent over the wave to establish whether or not a formed bead could withstand the wave solder process. Results confirmed that solder beads can not be successfully probed after being subjected to the wave solder process. The beads were reduced to a mere coating or tinning of the trace at the bead location.

3.4 Solder Beads

Defining the process for constructing reliably probeable solder beads within current PCB specifications was essential to avoid increased board manufacturing costs. Since specifications for solder mask thickness do not address the use of a trace as a solder surface, the required solder ball height needed to be achieved assuming the worst-case solder mask thickness limitations (1-mil minimum/2-mil maximum above the surface to be soldered).

Within this limitation and after being probed multiple times at ICT, the solder bead had to remain high enough to prevent the probe from making contact with the solder mask. Factors that could be critical to success included solder paste selection, design of the aperture on the solder paste stencil, and differing factory solder reflow conditions.

Goals

Assuming the worst-case solder mask thickness and registration tolerance, demonstrate that solder beads of sufficient height and mechanical reliability can be formed on the primary and secondary sides of boards representative of commonly used board geometries. Achieve this goal with no incremental material or design costs while addressing common manufacturing and material variables.

Test Methods

To simulate the minimum solder mask thickness, one coat was applied to both sides of the board. A standard stainless steel, 5-mil thick solder paste stencil was used with varying aperture shapes and sizes designed to yield a reflowed solder bead height that would be higher than the maximum solder mask height.

All the stencil apertures were larger than the exposed trace area to ensure sufficient height of the finished bead. [Figure 6](#) illustrates the size of the trace relative to the deposited paste.

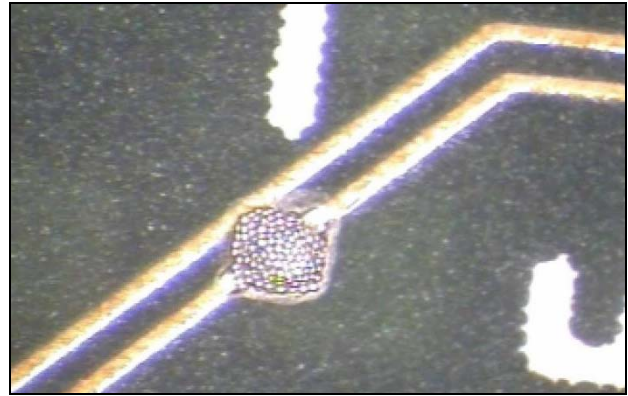


Figure 6. Example of solder paste printed over exposed trace prior to reflow soldering

Additional test variables included air versus nitrogen reflow oven atmospheres, different types of lead-free, no-clean solder pastes (SAC305 with flux A and SAC405 with flux B), and reflowed solder beads on both sides of the board. Contact resistance was characterized for all tested variables.

Results

Forming solder beads on traces and probing them at ICT presented no problems on boards that had multiple coats of solder mask. The design of the solder paste aperture provides a solder bead height that can accommodate thin and thick solder mask coatings on the board.

Figures 7 and 8 show sufficient solder bead height with nominal and worst case solder mask heights.

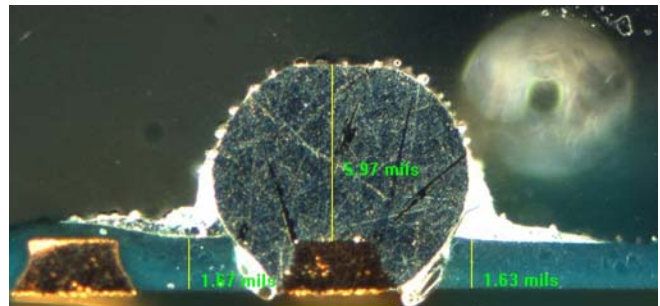


Figure 7. Unprobed solder bead with nominal mask thickness

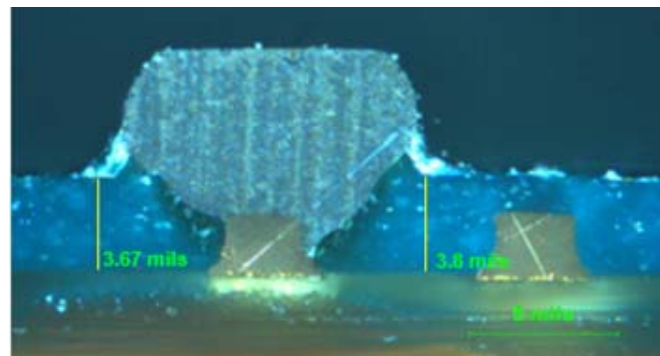


Figure 8. Probed solder bead with worst-case mask thickness

There was no statistical difference in solder bead contact resistance for the primary side, that gets reflowed once, and the secondary side, that gets reflowed twice. Reflow oven atmosphere and the metallurgical composition of the solder paste were also not significant. The type of flux used was critical, since the flux residue impacts

probe performance. The single coat of solder mask on the board surface yielded better results using flux A.

[Figure 9](#) shows the height of solder beads above the trace surface for solder mask offsets (N = - 3 mils, C = 0 mils, P = + 3 mils).

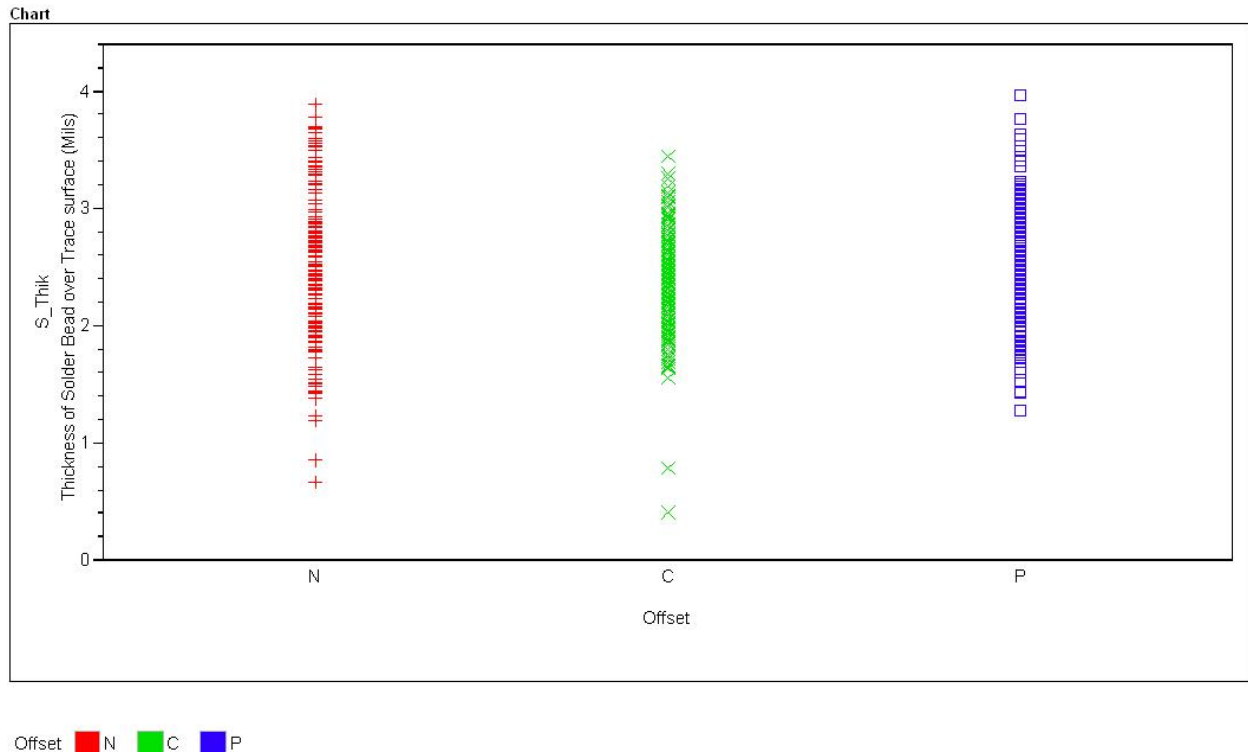


Figure 9. Solder bead height in mils as measured by AXI for nominal solder mask height

3.5 Trace Reliability

Commonly used PCB trace geometries—width, spacing, and angle on the board—together with worst-case solder mask misregistration, could conceivably reduce the solderable surface area of the exposed trace to a size that would prevent placement of a mechanically reliable solder bead. In addition, the possibility of mechanical degradation of the trace itself needed to be thoroughly investigated.

Goal

Demonstrate that mechanically reliable solder beads can be developed on traces representing typical orientation and space variations where the width of the exposed metal is less than the width of the trace. Show that subsequent probing at ICT, temperature cycling, and re-probing do not compromise any trace characteristics.

Test Methods

Every trace/space combination has 4 different orientations – 0, 45, 90 and 135 degrees with respect to the direction of travel of the squeegee used to apply solder paste. These were located in every square inch of the board. Boards were printed with solder paste and reflowed following standard factory procedures. The presence of solder beads on traces were then verified using X-Ray equipment before sending the board to ICT to measure contact resistance. The height of the solder bead above the trace surface was recorded so it could be correlated with contact resistance data.

Boards were tested up to ten times, simulating a factory worst-case process, then submitted to temperature cycling to stress the beads and traces. The boards were tested five more times after temperature cycling. Cross-sectioned board samples were then inspected for evidence of trace degradation and trace-to-FR4 bond quality.

Results

The orientation of the trace with respect to the direction of travel of the squeegee had no negative impact on the placement of solder beads; however, the width and the shape of the solder mask opening for a given trace width was critical. After the optimal opening was established, perfectly shaped solder beads were placed that provided good contact even with solder mask registration offsets.

The cross-sectioned sample in [Figure 10](#) shows a perfectly formed, unprobed bead, centered on the trace, with good height and bonding. The sample in [Figure 11](#) shows a second unprobed bead that only partially hits the trace due to mask offset. In similar cases, good probe contact was achieved.

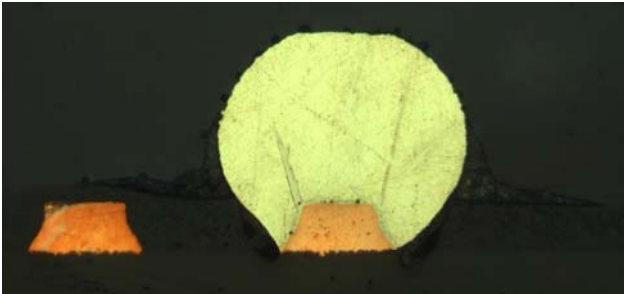


Figure 10. Unprobed bead with mask centered on trace

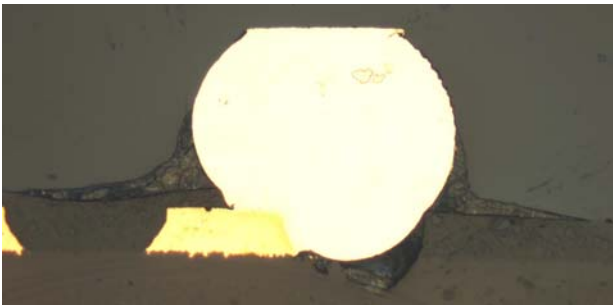


Figure 11. Probed bead with mask offset on trace

Neither the test process nor the subjection to stress and aging simulations had a negative impact on the trace. Figures 12 through 15 show different views of cross-sectioned samples after temperature cycling and ten probe hits. No cracks or separation of the trace from the FR4 were present.

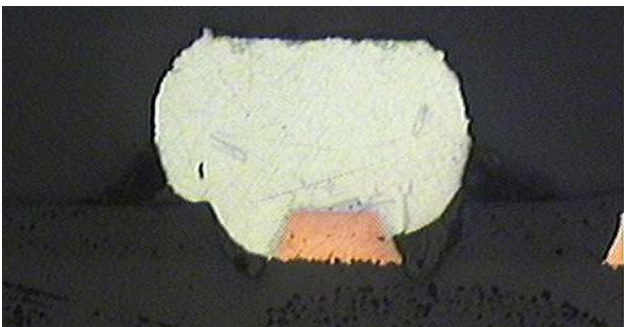


Figure 12. Latitudinal cross-section after aging and 10 probe hits

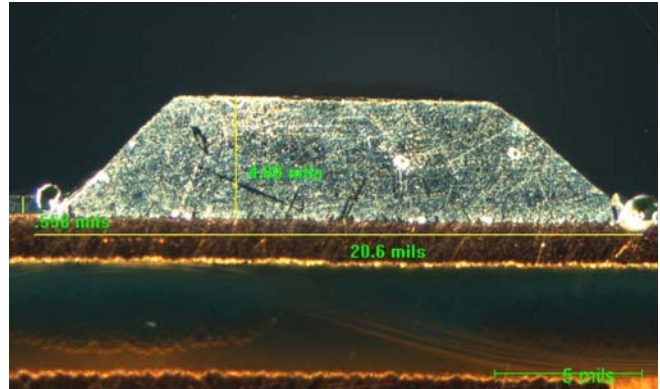


Figure 13. Longitudinal cross-section after aging and 10 probe hits

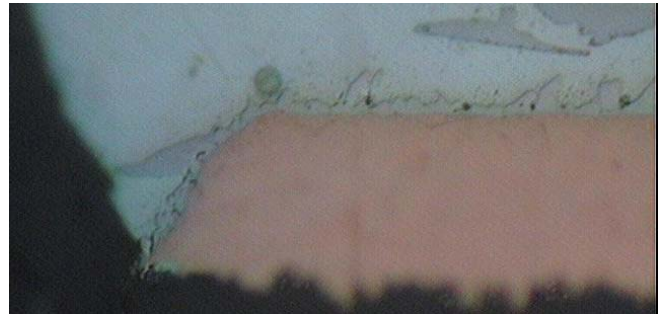


Figure 14: Left side close-up of solder bead and trace—no degradation after aging and 10 probe hits



Figure 15: Right side close-up of solder bead and trace—no degradation after aging and 10 probe hits

[Figure 16](#) and [Figure 17](#) show a highly magnified, inverted view of the same trace shown in [Figure 14](#), achieved using the Scanning Electron Microscope (SEM). No cracks are visible.

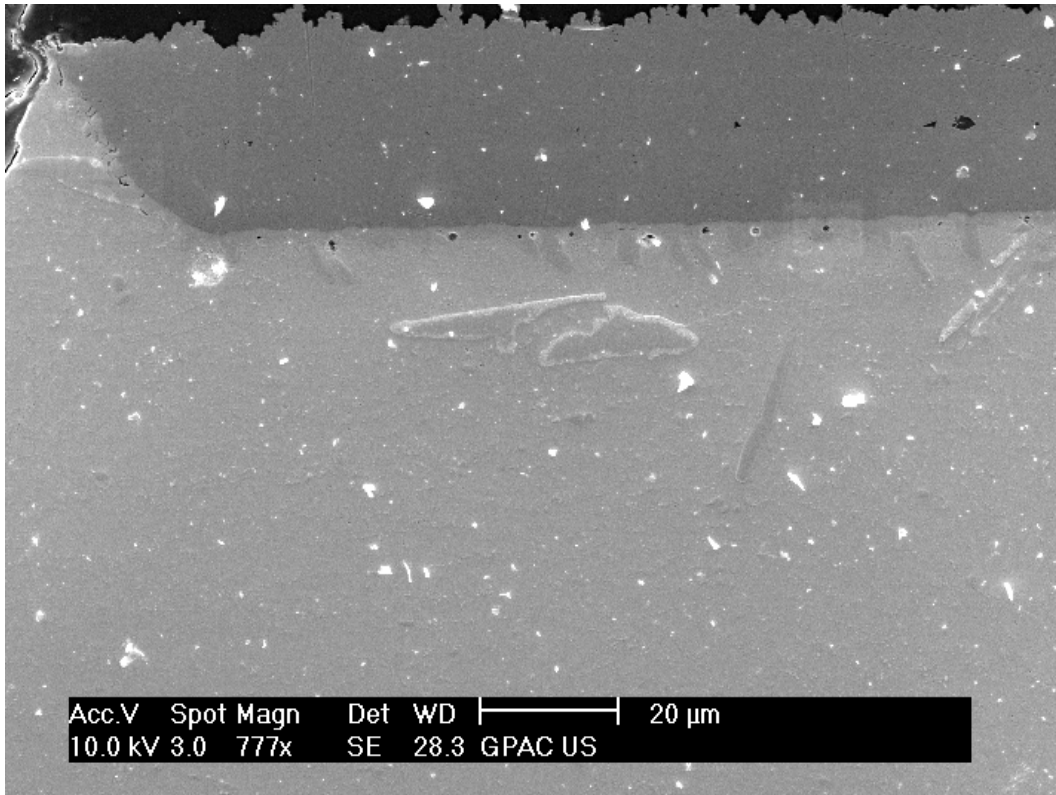


Figure 16. Inverted SEM view of the left side of the same trace shown in Figure 14—shows no cracks

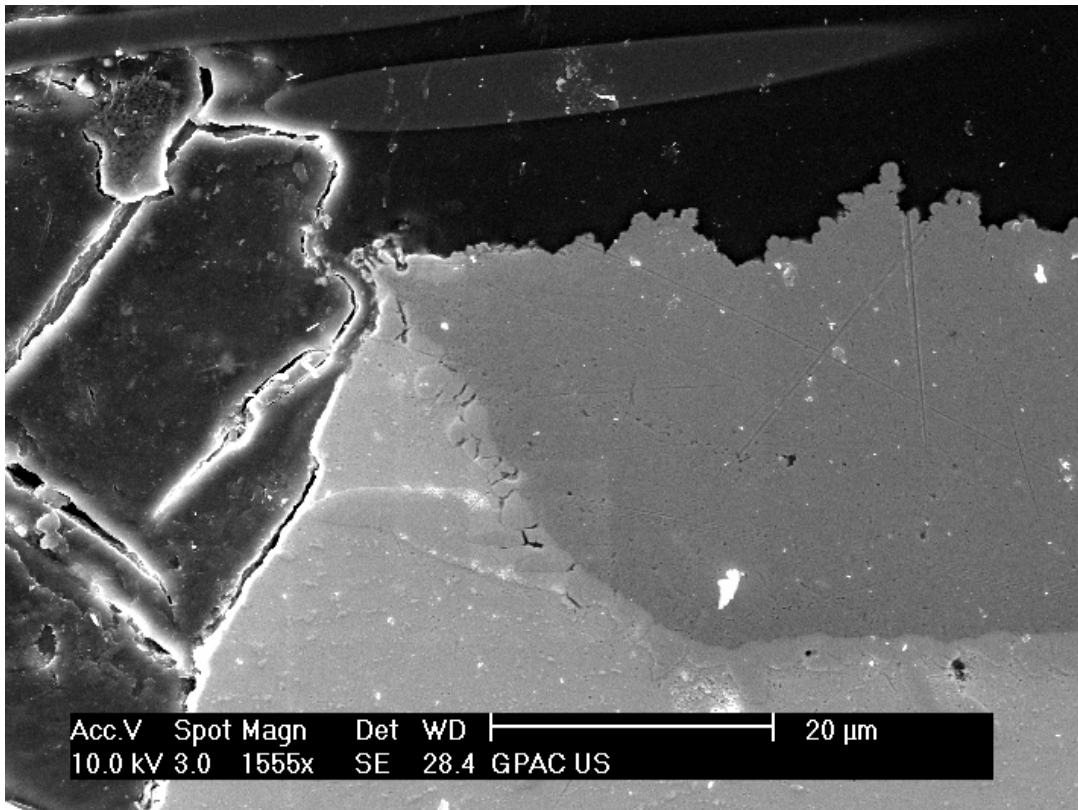


Figure 17. Inverted SEM view of the left side of the same trace shown in Figures 14 and 16—shows no cracks

3.6 Fixture Probes

Agilent studies [1] and [2] have established that solder beads require a flat-headed probe, but historically, this probe type has had poor success in penetrating flux and/or oxide build-up on testpoints. The study needed to determine whether probing solder beads reliably would require higher spring force than traditional testpoints in order to overcome contact resistance. We did not want to see increased stress on the board to achieve reliable contact.

Goal

Establish the optimal probe force for achieving 99.999% probability of contact.

Test Methods

Two different probe types were used: The flat-headed probe, a standard in use today, and a rotating variant of the flat-headed probe. The rotating probe was more expensive, but in theory it would improve flux and oxide penetration. Since a typical industry standard for traditional testpoint probing applies a spring force of 7.2 oz-Force (2 Newton), three probe forces, 2.0, 3.5, and 6.7 oz were tested. The rotating probe was tested using only the 3.5 and 6.7-oz forces.

A set of boards was tested using all five probe types. This generated over 300,000 data records per probe type.

Results

Figure 18 clearly indicates that the 6.7 oz flat-headed probe had the best results, met requirements, and performed better than traditional probing technologies. Note the exceptional mean of 0.0157 ohms (15.7 milliohms) for the 6.7 oz probe versus 0.157 ohms for the 3.5 oz and 20 ohms for the 2.0 oz (represented by the 3 circles in the figure). Traditional probing has a mean of 0.020 ohms. The standard deviation for the 6.7 oz was 0.010 ohms (versus 6.25 ohms for 3.5 oz probes and 756 ohms for the 2.0 oz).

There was no significant difference between the rotating and non-rotating versions, but this data is not shown in Figure 16.

The success of the 6.7 oz probe also means that less force and consequently less strain is applied to the board.

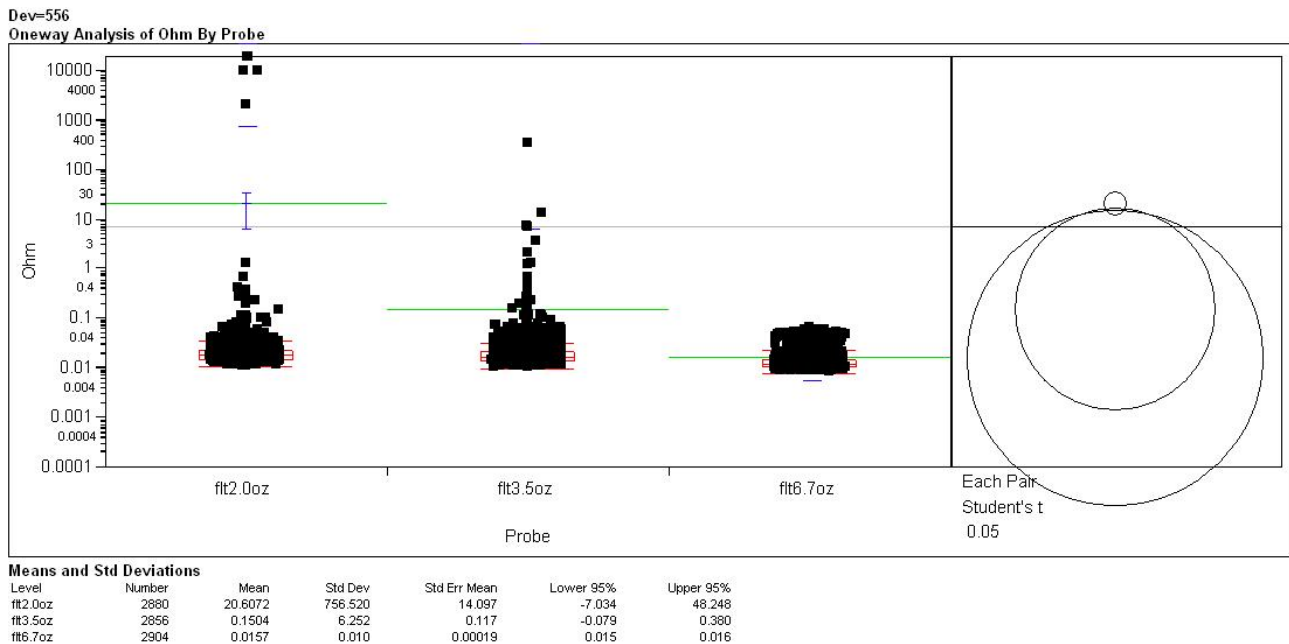


Figure 18. Analysis of contact resistance by probe

3.7 Test Process

In manufacturing test and repair environments, boards must withstand multiple tests, which involves many fixture activations. Boards of varying ages returning from the field for repair must also be testable.

Goal

Determine the impact on solder-bead probing when boards are retested many times under conditions that are likely to occur.

Test Method

Two methods were used: First, a worse-case HVM factory retest of five times per board was applied under three likely conditions: immediately after manufacture (new), after storing for several days, and after a humidity bake to simulate aging. All five probe types were used under each test condition. Second, to determine if there was a break point, one board was subjected to 100 tests.

The humidity bake was at 85°C and 85% relative humidity. One batch of boards was baked for 72 hours, simulating aging of six months; a second batch was baked for 300 hours, simulating aging of two years.

Results

In [Figure 20](#), data collected for the 6.7-oz probe shows no significant increases in contact resistance during the five test runs for the high volume manufacturing simulation. Note that with each consecutive run, the contact resistance trends down.

[Figure 19](#) shows test results for new boards (blue line), boards subjected to a 72-hour bake (magenta line), and board subjected to a 300-hour bake (red line). New boards were each tested five times, baked for 72 hours, then retested five more times. They were then baked for a total of 300 hours and retested five more times.

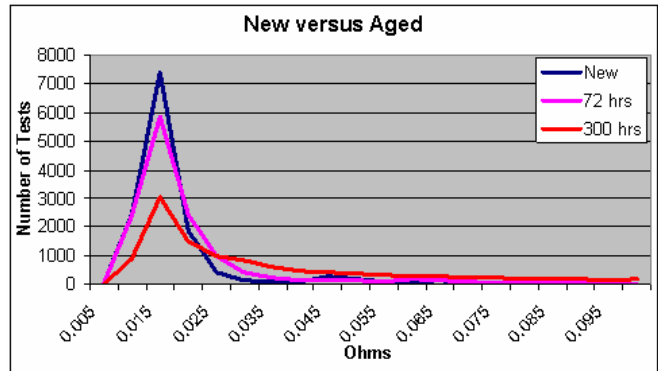


Figure 19. Newly manufactured versus aged boards

The graph data shows no statistically significant difference in contact resistance after the 6-month aging simulation; however, contact resistance distribution did increase for the 2-year aging. Increasing the probe spring force to 8 and 10 oz did not improve the contact resistance.

Performance data for traditional probe techniques under the same circumstances was not available, so no valid comparison could be made. However, a higher retest rate for boards returned after two years was not considered an issue, given that it would be low volume and may not be tested by ICT.

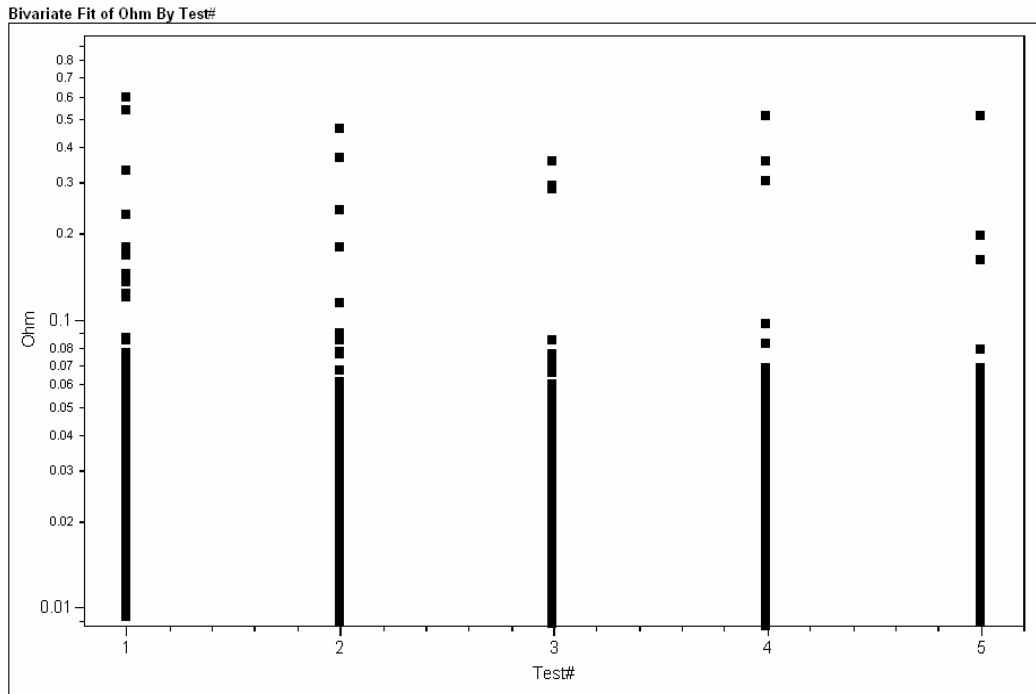


Figure 20. Contact resistance for tests 1 - 5

4 CAD tools

There have been no issues applying the existing capability of major commercial CAD suppliers to PCB designs using solder-bead probing. No enhancements or utilities are needed.

5 Future Work Planned

Two extensions of this study are currently underway. The first will characterize the signal integrity on differential traces. The second will characterize the probe performance for different surface finishes and for several different solder pastes (flux sensitivity) that are used world wide. Both experiments are expected to be completed by the end of 2006.

6 Conclusion

PCB Design Engineers, CAD Designers, and ICT Engineers have every reason to be excited about the results of this study. Over 1.5 million data points lead us to believe that solder-bead probing is not only feasible in a high volume production environment, but can be successfully implemented without any increase in cost or restrictions to design flexibility. Particularly encouraging is the data showing no impact to signal integrity. The potential to improve test coverage and efficiency in a demanding product environment is also evident.

Intel has begun to implement solder bead probing technology on future platforms.

7 Acknowledgements

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8 References

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- [2] K. P. Parker, "Bead Probes in Practice," *Proceedings IEEE International Test Conference*, 2005